

# DW750 Installation Guide

Prepared by Educational Services  
of  
Digital Equipment Corporation

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UNIBUS	VAX	RSX
	VMS	IAS

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## INSTALLATION

### INSPECT PARTS

The basic DW750 option consists of the following hardware parts. Check to be sure that none are missing or damaged before you procede.

Quantity	Description
1	L0010 Second UNIBUS(SUB) Module
1	Ribbon cable assembly consisting of:  (3) 40-conductor BC06 ribbon cables, tie wrapped and formed.
1	M9014 Transition module
1	M9302 UNIBUS Terminator

There should be an expansion box, and possibly an expansion cabinet. The expansion box and/or cabinet are not part of the DW750 option, but should have been ordered separately.

## INSTALL EQUIPMENT

1. Check the hardware revision level and power the system down.
  - a. If VMS is running, bring it down. Either have the customer bring it down, or with his permission type the following command.  
  

```
$ @sys$system:shutdown
```
  - b. Examine the CPU hardware revision level to ensure compatibility between the option and the CPU. If the CPU is not at the correct revision level, do not proceed with this option installation until the CPU is updated and checked out. The following example shows you how to check the CPU rev.  
  

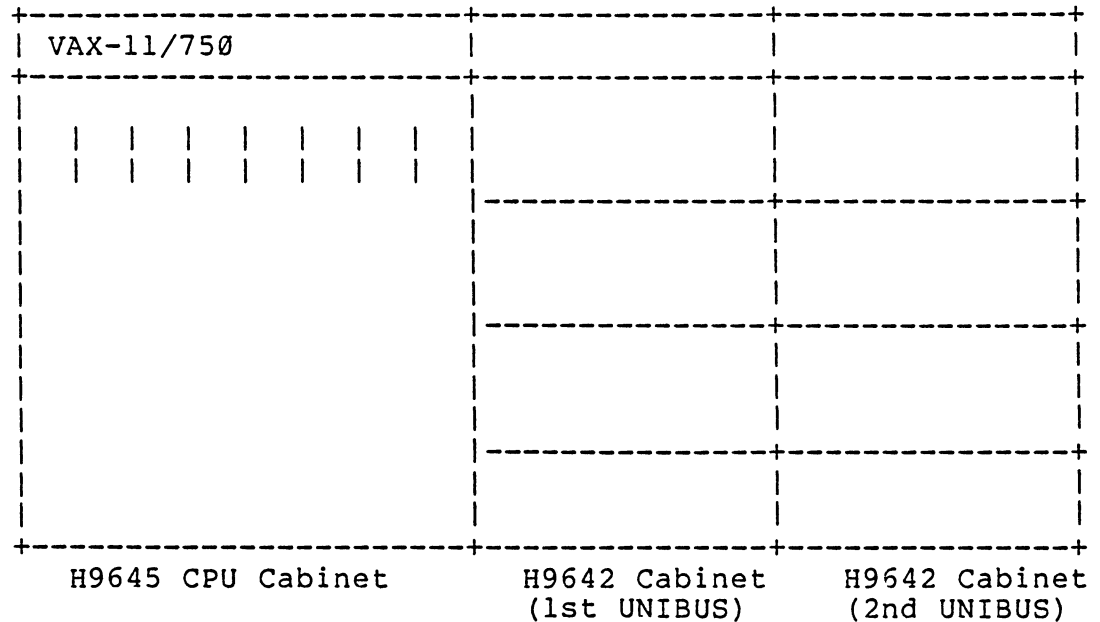
```
>>> E/I 3E
```

```
      I  0000003E      02005E30
(for systems with 16K arrays)
      OR
      I  0000003E      02005E48
(for systems with 1meg arrays)
```
  - c. Use the key switch to power the system off.

- EXAMPLE 1:



EXAMPLE 2:



3. Set up the VELOSTAT Kit.
  - a. Unfold the VELOSTAT mat to full size (24x24).
  - b. Attach the 15' ground cord to the VELOSTAT snap fastener on the mat, and the alligator clip of the ground cord to a good ground on the VAX-11/750.
  - c. Attach the wrist strap to either wrist and the alligator clip to a convenient portion of the mat.
4. Unpack the L0010 module.
  - a. Place the L0010 module while still in the box on the VELOSTAT mat.
  - b. Remove the module from the box and protective covering and lay it flat on the VELOSTAT mat. This will bring the module to the same potential as the CPU and eliminate static discharge damage.



5. Install the DW750 option.

- a. With the wrist strap still attached to your wrist, install the L0010 module in a CMI option slot. The first CMI option slot is recommended (VAX-11/750 slot number 7) to alleviate cabling problems.
- b. Remove grant jumpers from backplane slot where L0010 is installed. No jumpers need to be added to the DW750 option because it has fixed addresses and a fixed CMI Arbitration Level of 3.

NOTE

RH750s start with CMI arbitration level (3). If you have one or more in your system, you must move them down one CMI arbitration level.

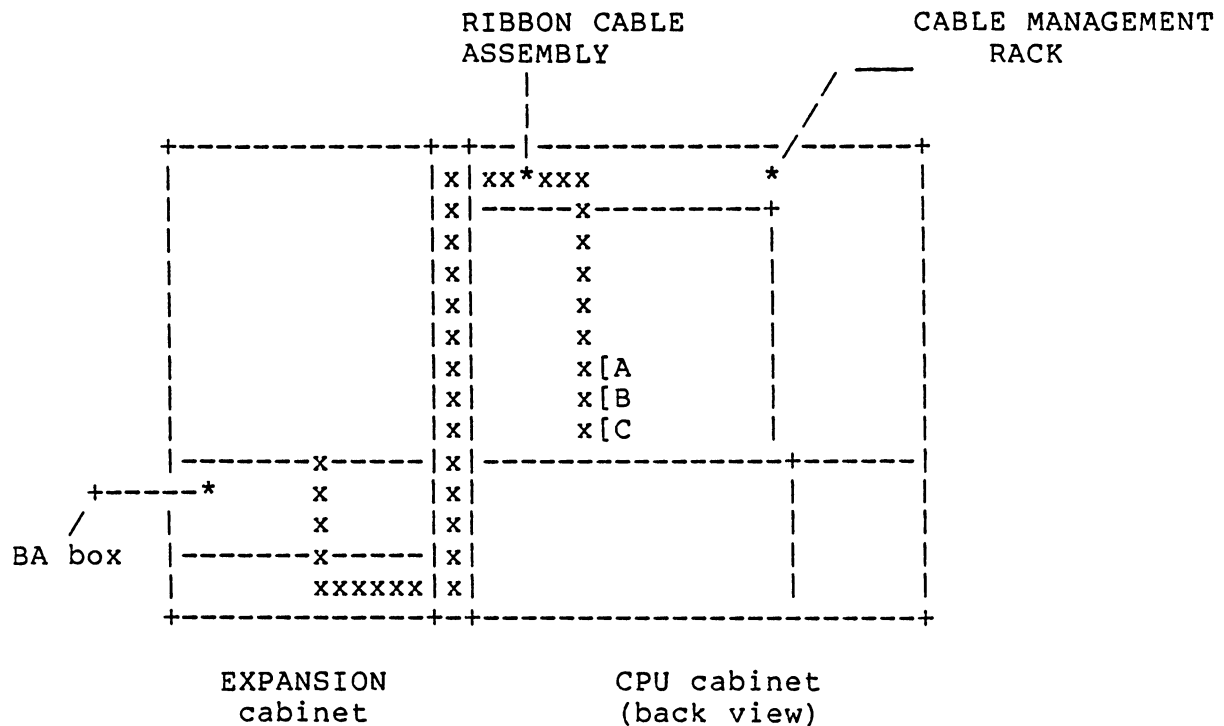
Without DW750 installed:

RH750 0 ADDRESS F28000 CMI ARB LEVEL 3  
RH750 1 ADDRESS F2A000 CMI ARB LEVEL 2

With DW750 installed:

RH750 0 ADDRESS F28000 CMI ARB LEVEL 2  
RH750 1 ADDRESS F2A000 CMI ARB LEVEL 1

- c. Connect the three ribbon cables to backplane slots B and C as in the MASSBUS option.
- d. Route the cable assembly up the backplane to the cable the VAX-11/750 CPU cabinet, and the expansion cabinet, then across the bottom of the expansion cabinet and up the back to the BA box (see diagram).



- e. Install the M9014 on the end of the cable in the UNIBUS IN slot of the expansion DD11 backplane.
- f. Install the UNIBUS options that are going on the second UNIBUS following their installation manuals.
- g. Install the M9302 UNIBUS Terminator module in slot AB of the last DD11 backplane.
- h. Install the UNIBUS Exerciser (UBE) module (M7855) from your Field Service Spares Kit into an SPC slot in the expansion DD11 backplane. Remove the NPG jumper wire (CA1 to CB1) in the backplane slot where the UBE is located.

NOTE  
UBE ADDRESS MUST BE SET FOR 770000 AND  
VECTOR SET FOR 510

SWITCHES	ADDRESS (E 125)	VECTOR (E 88)
S1	ON	ON
S2	ON	ON
S3	ON	ON
S4	ON	ON
S5	ON	OFF
S6	ON	OFF
S7	ON	ON
S8	ON	OFF

6. Check for power and ground shorts in the expansion box.
7. Check the remote sense cable. Make sure the remote sense cable is connected from the CPU to the expansion cabinet.
8. Power the system on.
  - a. Turn on all breakers.
  - b. Turn on key switch.

## HARDWARE CHECKOUT

1. Examine the buffer data path registers of the second UNIBUS.

There are three buffer data path registers, and they are at the following addresses.

CSR1    F32004  
CSR2    F32008  
CSR3    F3200C

EX:

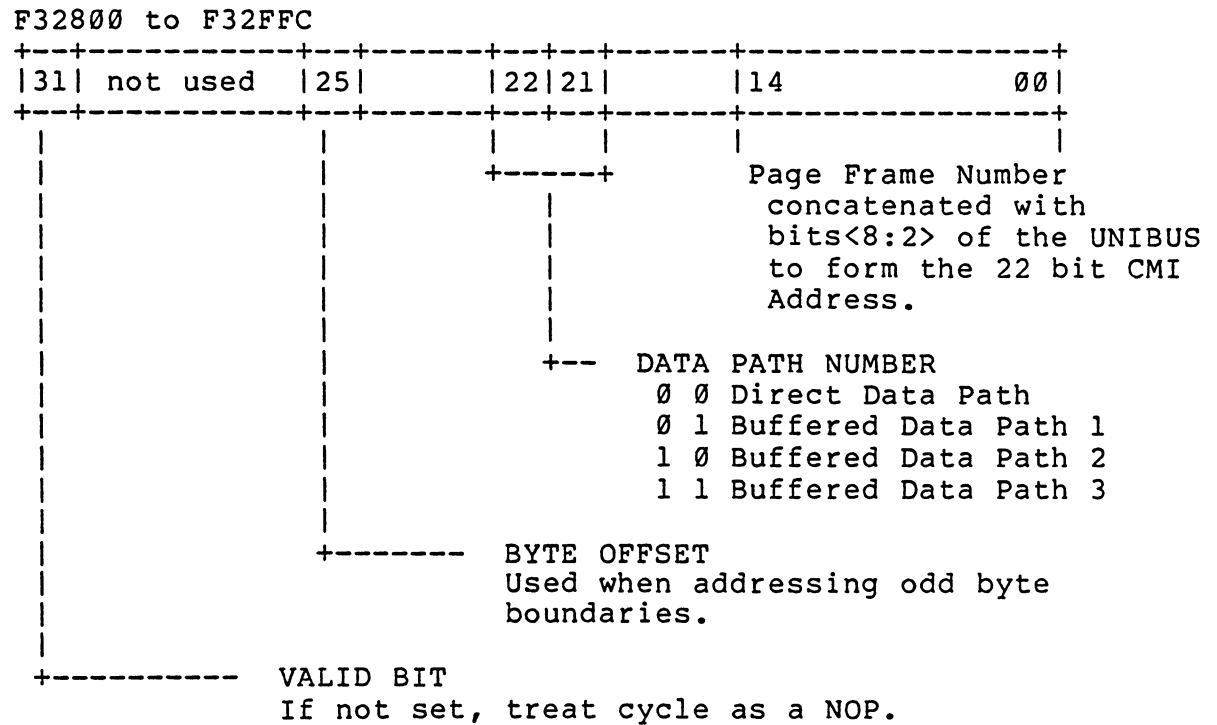
>>> E/P F32004

The register format of each of the registers is as follows.

31	30	29	28	-- not used --																01	00
			(PUR) Purge Request																		
			(UCE) Uncorrectable Error																		
			(NXM) Non Existent Memory																		
			(ERR) Error Flag [OR of bits 29 & 30]																		

2. Examine some of the second UNIBUS map registers.

They fall into the addresses between F32800 and F32FFC and the registers have a format as follows.



### 3. Examine the IPEC registers.

- a. These registers are similar in function to the UET registers module, but accessed through the Second UNIBUS. Therefore, if you can examine these registers you have proven you can access the Second UNIBUS and it is not hung.

IPEC REGISTERS	CMI ADDRESS	UNIBUS ADDRESS
Address register	FBF460	772140
Data register	FBF462	772142
Control register 1	FBF464	772144
Control register 2	FBF466	772146

EX:  
>>> E/W/P FBF460

NOTE  
When examining or depositing these registers, use Word Length Format rather than Long Word Format.

EX: E/W FBF460

- b. The following is a description of the IPEC registers:

```

ADDRESS REGISTER  FBF460
+-----+
|15                                           00|
+-----+

```

This register contains sixteen of the address bits used during an NPR transfer initiated by control register 1. The upper two bits, 16 and 17, are contained in control register 1.

```

DATA REGISTER  FBF462
+-----+
|15                                           00|
+-----+

```

This register has a dual function. For an NPR cycle it contains the data either sent or received by the NPR. For a BR cycle it contains the vector passed with the interrupt.

CONTROL REGISTER 1 FBF464

+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+															
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00															
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+															
I	I	A	A	B	B	B	B	P	T	P	A	A	C	C	N
N	N	C	C	R	R	R	R	E	O	B	1	1	1	0	P
I	T	L	I	7	6	5	4				7	6			R
T	D	O	E												
	O	1													
	N														
	E														

NPR - Setting this bit causes the device to do an NPR cycle with the data contained in the address and data registers. If the bit fails to clear, it indicates that the device was unable to become bus master. This bit is also cleared by INIT.

C0, C1 - These bits determine what type of transfer will be done when NPR is set. They are as follows.

C1	C0	
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

A17, A16 - These bits are the upper two bits of the address register. INIT does not clear these bits.

PB - Setting this bit simulates a memory parity error setting the BUS PB signal on the UNIBUS when the data register is read. This bit is cleared by INIT.

TO - This bit indicates that a UNIBUS transfer timed out and SSYN was not returned. It is reclocked every transfer, and cleared by INIT. READ ONLY.

PE - This bit indicates that BUS PB on the UNIBUS occurred during a DATI. It is reclocked every DATI cycle, and also cleared by INIT. READ ONLY.

BR7-BR4 - These four bits cause the device to assert their respective BR requests, and attempt to interrupt at that level. They may be set in any combination to verify the arbitration logic. Once these bits are set the IPEC will attempt to interrupt until either the bit is cleared or the interrupt has taken place. These bits are not cleared by the interrupt taking place, and must be explicitly cleared by either writing a zero to the appropriate bit position, or by INIT before they can be set again to initiate another interrupt.

ACIE - This bit is ACLO Interrupt Enable. When set, it will cause an interrupt to vector 1E4 on the leading edge of a UNIBUS ACLO signal (power going down) and again approximately 100 ms after the trailing edge of ACLO (power coming up). Cleared by INIT.



ACLO1 - This bit is set by a power fail condition, and causes an interrupt if ACIE is set. READ ONLY

INTDONE - This bit indicates an interrupt has taken place that was caused by one of the BR bits being set. The bit is cleared by writing a (1) to it or by INIT.

INIT - This bit will initialize the internal logic of the IPEC when set. The output is undefined when read.

#### CONTROL REGISTER 2 FBF466

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
E	I	A	B	B	B	B	V	V	V	V	V	V	V	V	V
X	N	C	R	R	R	R	8	7	6	5	4	3	2	1	0
T	T	L	7	6	5	4									
M	D	O													
O	O	2													
D	N														
E															

V8-V0 - These bits specify the vector to be used by an interrupt initiated by Control Register 2. These bits are NOT cleared by INIT.

BR7-BR4 - These bits cause the device to interrupt in the same manner as the BR bits in Control Register 1. Cleared by INIT.

ACLO2 - This bit when set will cause ACLO on the UNIBUS to be asserted for approximately 1.5 ms. The bit is self clearing. This bit is NOT affected by INIT.

INTDONE - This bit works the same as the INTDONE bit in Control Register 1, but for interrupts initiated by the BR bits in Control Register 2. This bit is cleared by writing a one to it or by INIT.

EXTMOD - This bit is reserved for future use, should be zero when read. READ ONLY.

4. Examine a UNIBUS exerciser register.

Examine location FBF000, this will give you location 770000 on the second UNIBUS. For a description of what the bits in the UBE registers do, consult the UBE User's Manual.

By examining a UBE register you are checking to be sure that you can get out to the BA box.

5. Boot up the diagnostic supervisor in standalone mode.

Minimum revision of the Diagnostic Supervisor that can be used is (6.4).

EX: B/10 XXXX

Where (XXXX) is the boot device.

6. Attach the DW750.

This can be accomplished either by running the Autosizer program EVSBA or by performing a manual attach.

EX:1

DS> RUN EVSBA

DS> SELECT ALL

EX:2

DS> ATTACH DW750 CMI DW1

DS> ATTACH UBE DW1 UB0 770000 510

DS> SELECT DW1

DS> SELECT UB0

7. Run the UBI/DW750 diagnostic.

A minimum of two passes of this diagnostic should be run. The program is called ECCBA, and should be REV 1.3 or higher.

EX:

DS> RUN ECCBA

8. Run appropriate diagnostics for devices on the second UNIBUS.

Run whatever other appropriate diagnostics are necessary to verify the peripherals that were added to the DW750'S UNIBUS. These diagnostics can be determined by referring to the installation manuals for the added devices, looking them up in EVNDX, or by using the Diagnostic Supervisor help file as follows.

EX:

DS> HELP DEV XXXX

Where (XXXX) is the device you want know about.

9. Remove the UNIBUS exerciser module.

- a. Remove the UBE module.

- b. Replace the NPG jumper wire on the backplane (wire from pins CA1 to CB1 in slot where M7855 is installed).

- c. Replace the Grant card back in its original slot (slot D of an SPC slot).

10. Bring VMS up and run UETP.

For information on setting up and running UETP refer to the VAX/VMS UETP User's Guide (AA-D643A-TE)

11. Return the system to the customer.

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